BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC1270H

T-74-05-01

30-50 W POWER AMPLIFIER DRIVER

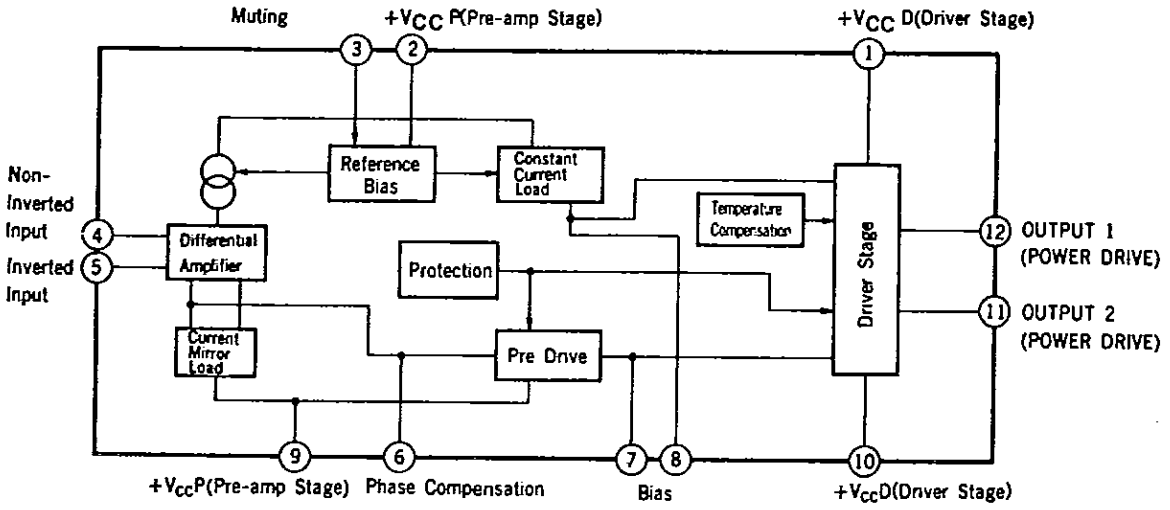
DESCRIPTION

μPC1270H is designed for use with a Hi-Fi power amplifier driver. It is composed of a differential amplifier, a predriver, a driver and protection circuit.
It is in a 12 pin small power SIP. (Single In Line)

FEATURES

- Excellent Low Distortion.
  0.002 % TYP. (V_{CC} = ±36 V, f = 1 kHz, A_v = 30 dB, P_O = 30 W, R_L = 8 Ohms)
  0.006 % TYP. (V_{CC} = ±36 V, f = 20 kHz, A_v = 30 dB, P_O = 30 W, R_L = 8 Ohms)
- Wide Frequency Band.
  900 kHz TYP. (-3 dB)
- Wide Power Band Width.
  90 kHz TYP. (P_O = 25 W, T.H.D. = 0.1 %)
- Excellent Low POP ON/OFF Noise.

BLOCK DIAGRAM



NOTE: The protection circuit is for this IC and cannot protect external Power Transistors. Thus, design a P_O Tr protection circuit besides.

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ABSOLUTE MAXMUM RATINGS (T_a = 25 °C)

Supply Voltage (Quiscent)	V_{CC1}	±50	V
Supply Voltage (Operational)	V_{CC2}	±45	V
Quiscent Circuit Current	$I_{CC\ (peak)}$	200	mA
Allowable Package Dissipation	P_D	4.1	W
Operational Temperature	T_{opt}	−20 to +75	°C
Storage Temperature	T_{stg}	−40 to +150	°C

RECOMMENDED OPERATING CONDITION

Supply Voltage (Operational)	V_{CC} = ±18 to ±36 V at MAX. Power Output
Input Bias Resistance	R_{IN} = 1 to 50 to 100 kohms
Power Transistor h_{FE}	h_{FE} = 50 at MAX. Power Output
Closed Loop Voltage Gain	A_v = 26 to 30 dB

ELECTRICAL CHARACTERISTICS (V_{CC} = ±36 V, A_v = 30 dB, Use Standard Test Circuit, T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITION
Output Offset Voltage	V_{OFF}		±5	±100	mV	SEE TEST CIRCUIT 1
Quiscent Circuit Current	I_{CC}		20	40	mA	V_{IN} = 0
Maximum Output Voltage	V_{OM}	20	23		V	T.H.D. = 0.05 % f = 20 to 20 kHz
Open Loop Voltage Gain	A_{VO}	80	95		dB	V_O = 1.5 V, f = 1 kHz
Output Noise Voltage	V_{NO}		0.07	0.14	mV	R_G = 10 kohms
Power Band Width	P.B.W.		900		kHz	V_O = 1.5 V, −3dB
Supply Voltage Rejection Ratio	S.V.R.	55	70		dB	R_G = 2 kohms, f = 100 Hz
Output Offset Voltage (Mute)	$V_{OFF\ (Mute)}$			±50	mV	V_{CC}=±50 V, TEST CIRCUIT 7

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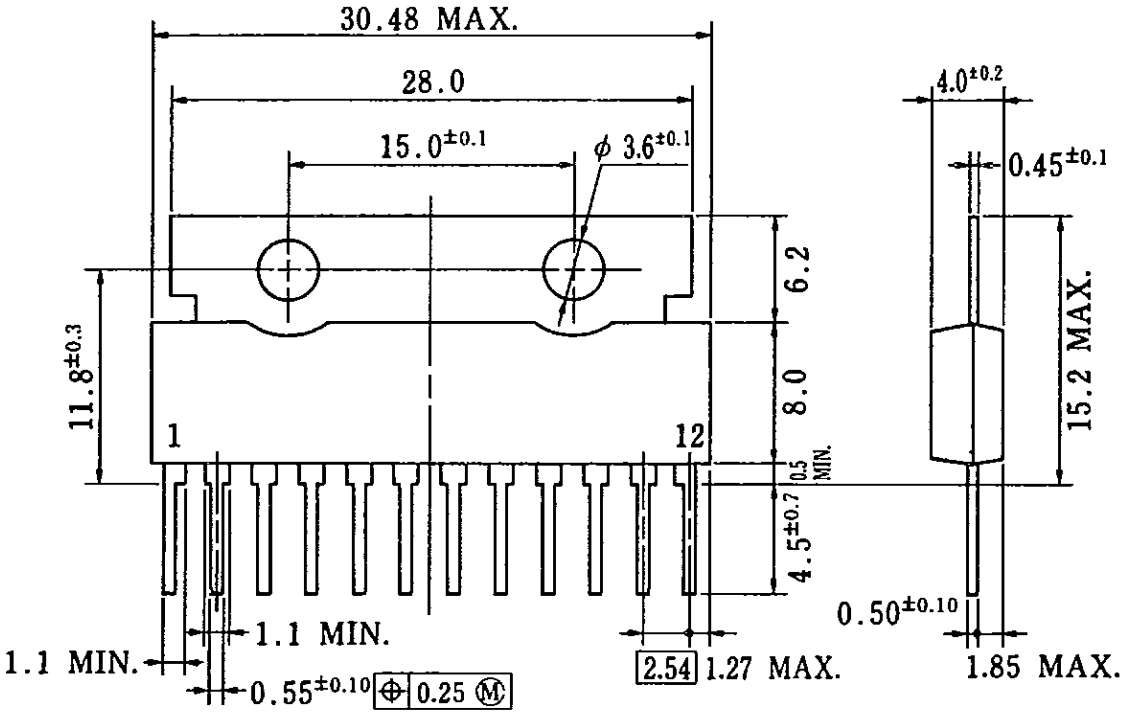
12 PIN SIP (Unit : mm)



P12HP-254B1

PIN CONNECTION DIAGRAM

PIN NO.	PIN CONNECTION
1	$+V_{CCD}$ (for Driver)
2	$+V_{CCP}$ (for Preamp)
3	MUTING
4	INPUT
5	NFB
6	PHASE COMP
7	BIAS
8	BIAS
9	$-V_{CCP}$ (for Preamp)
10	$-V_{CCD}$ (for Driver)
11	LOWER OUTPUT
12	UPPER OUTPUT

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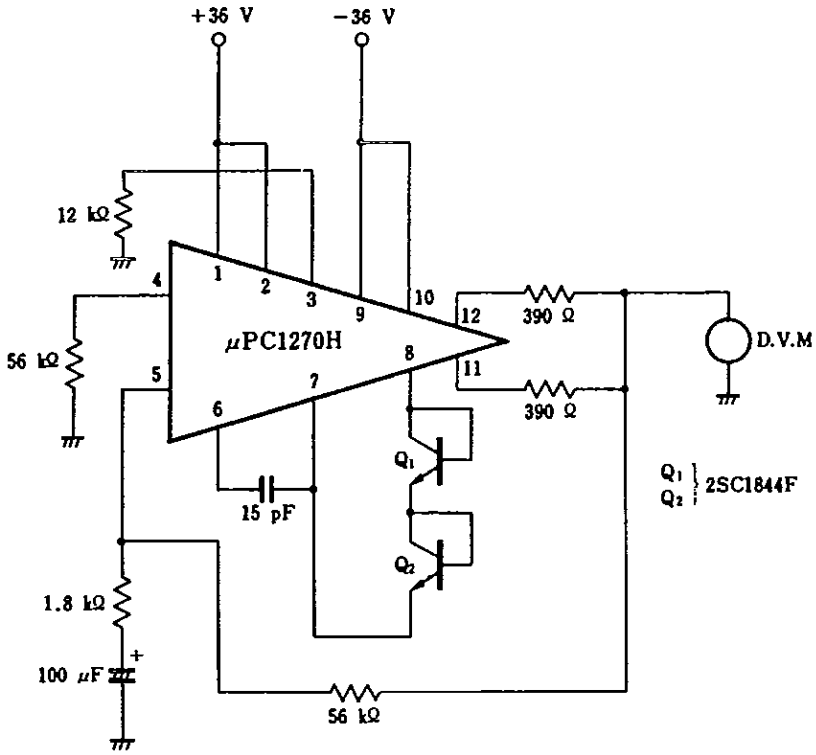
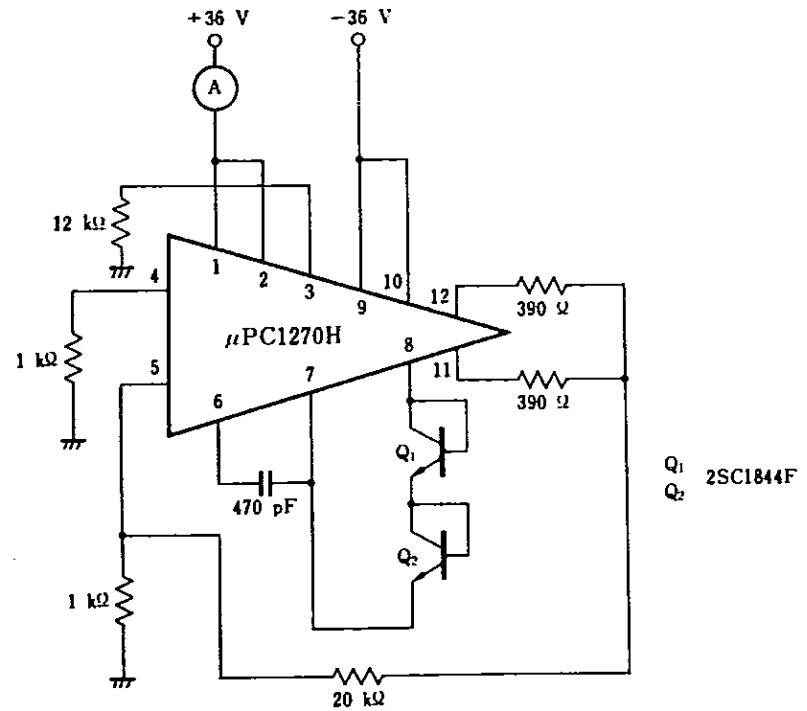
TEST CIRCUIT 1 (V_{OFF})



TEST CIRCUIT 2 (I_{CC})



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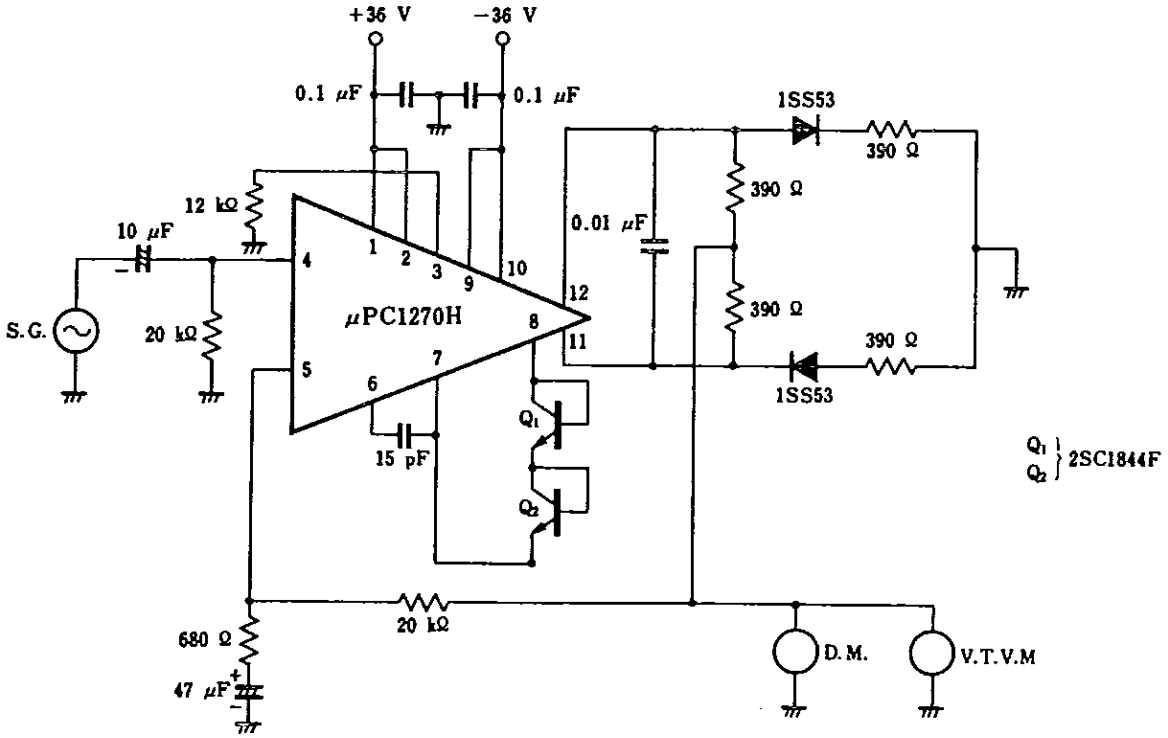
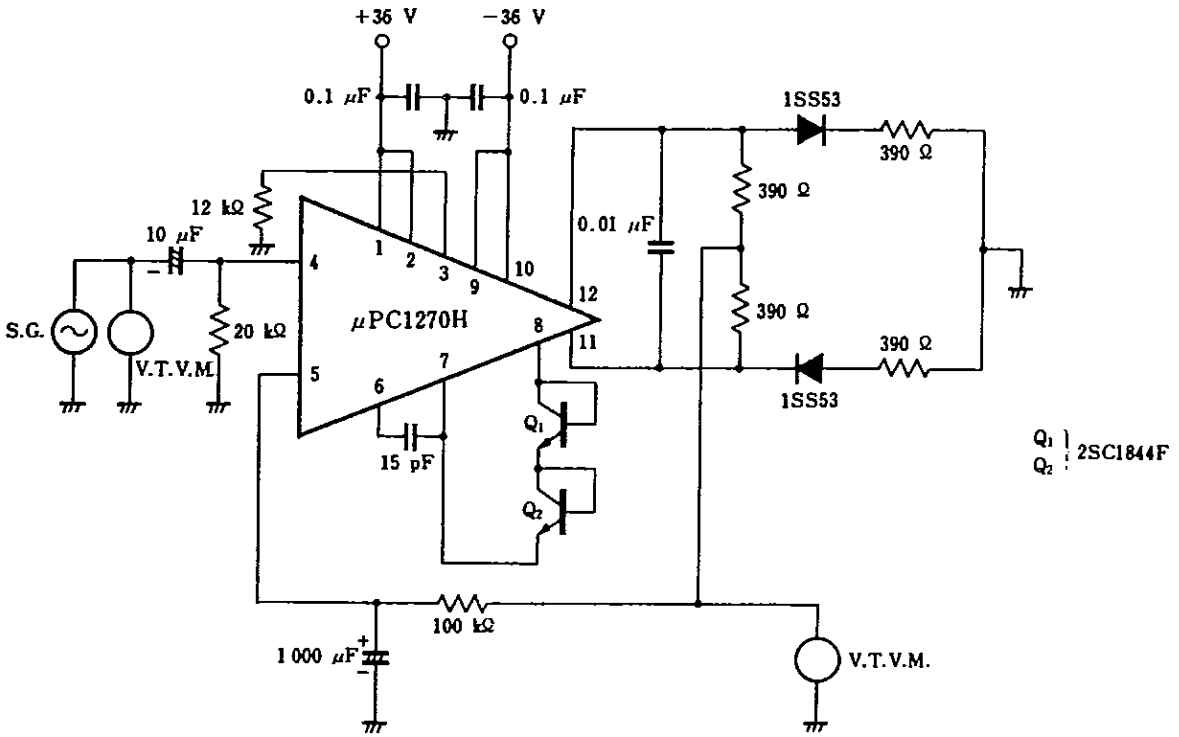
TEST CIRCUIT 3 (V_{OM})



TEST CIRCUIT 4 (A_{VO})



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TEST CIRCUIT 5 (V_{NO})

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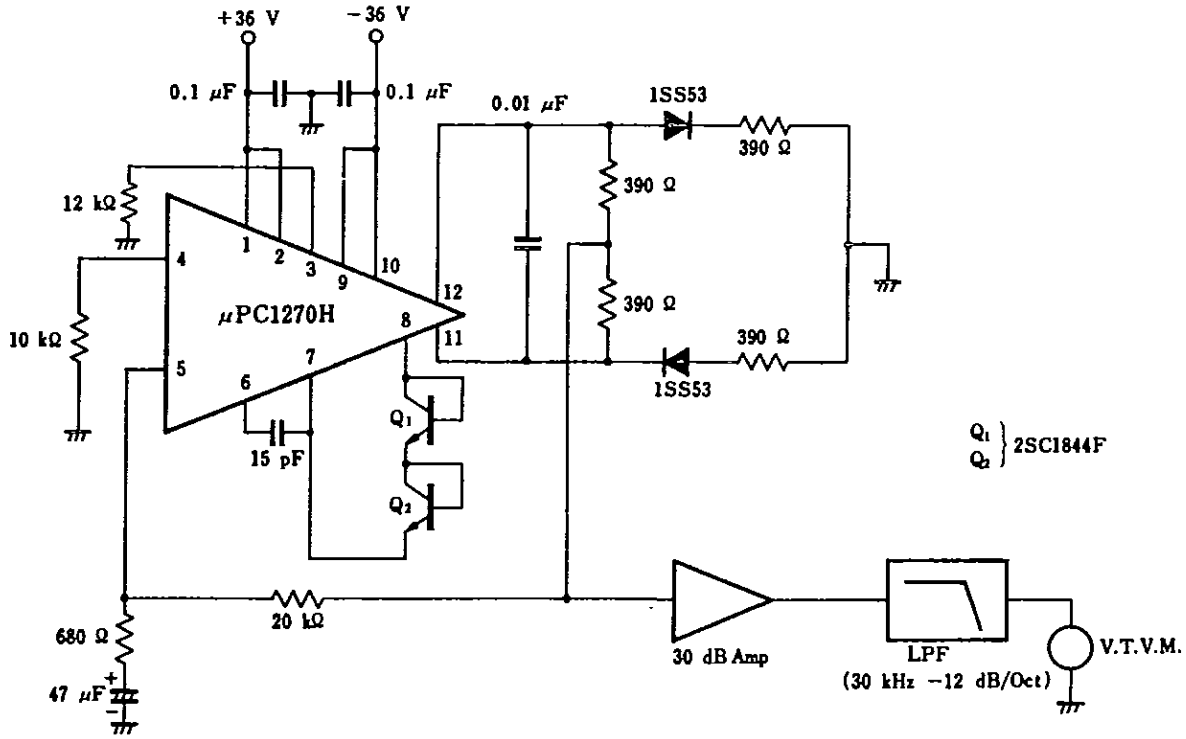
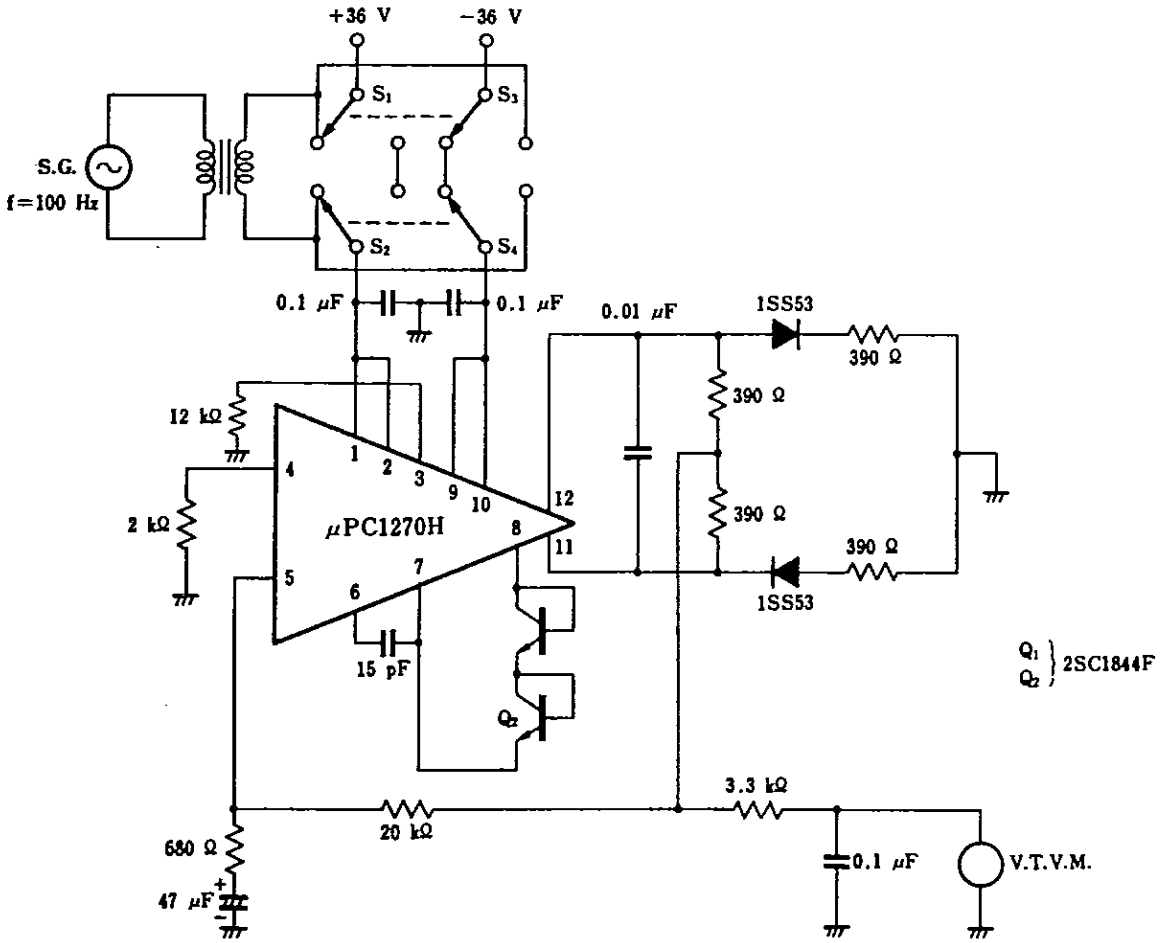


TEST CIRCUIT 6 (S.V.R.)



TEST CIRCUIT 7 ($V_{OFF(MUTE)}$)

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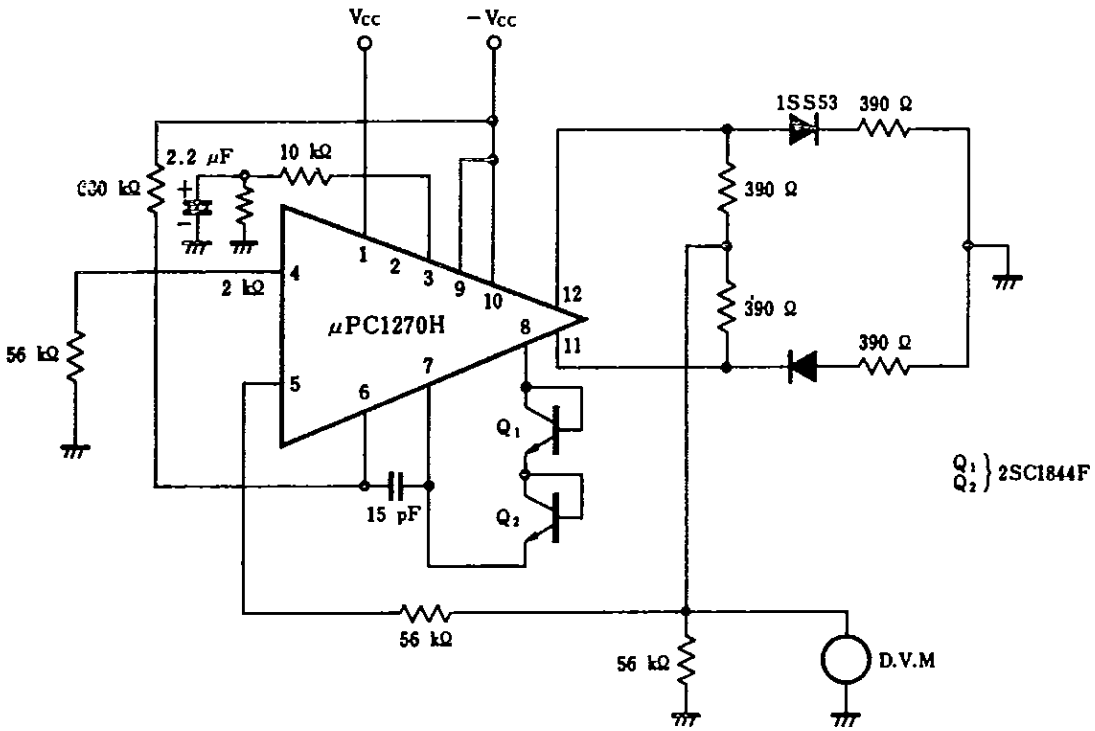

TYPICAL CHARACTERISTICS (Ta = 25°C)

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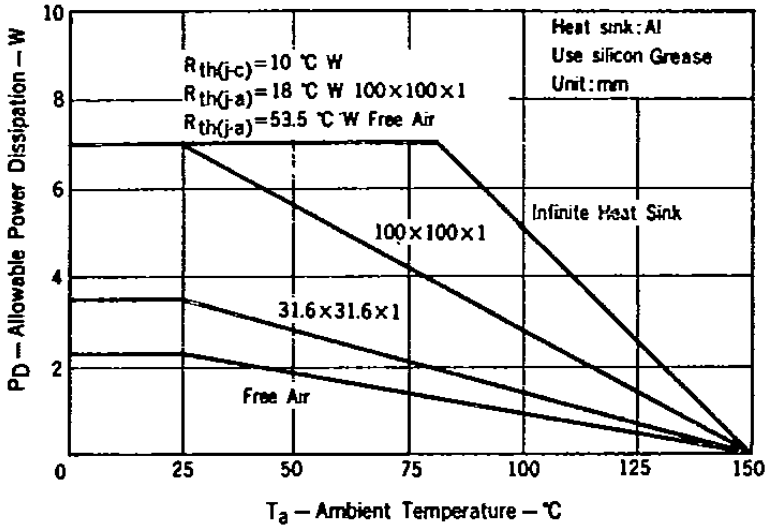
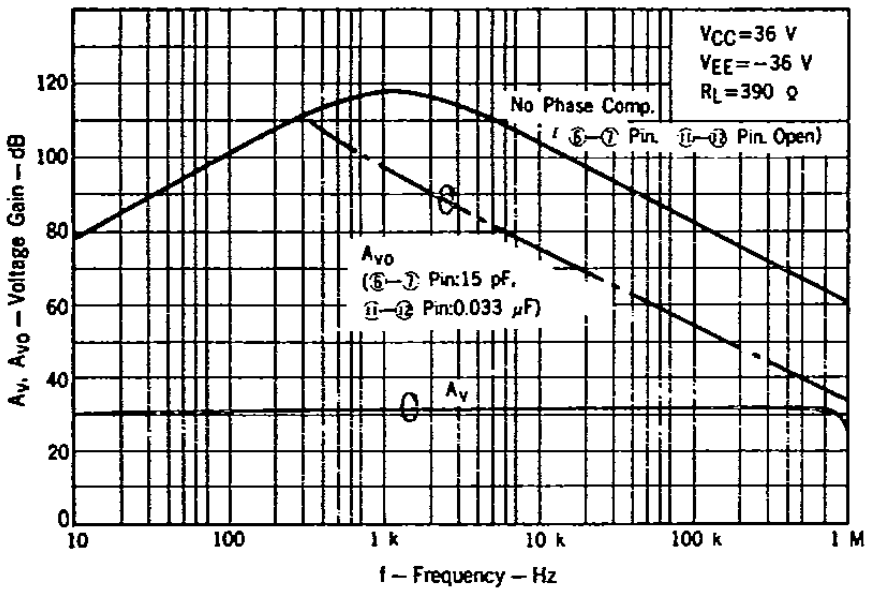
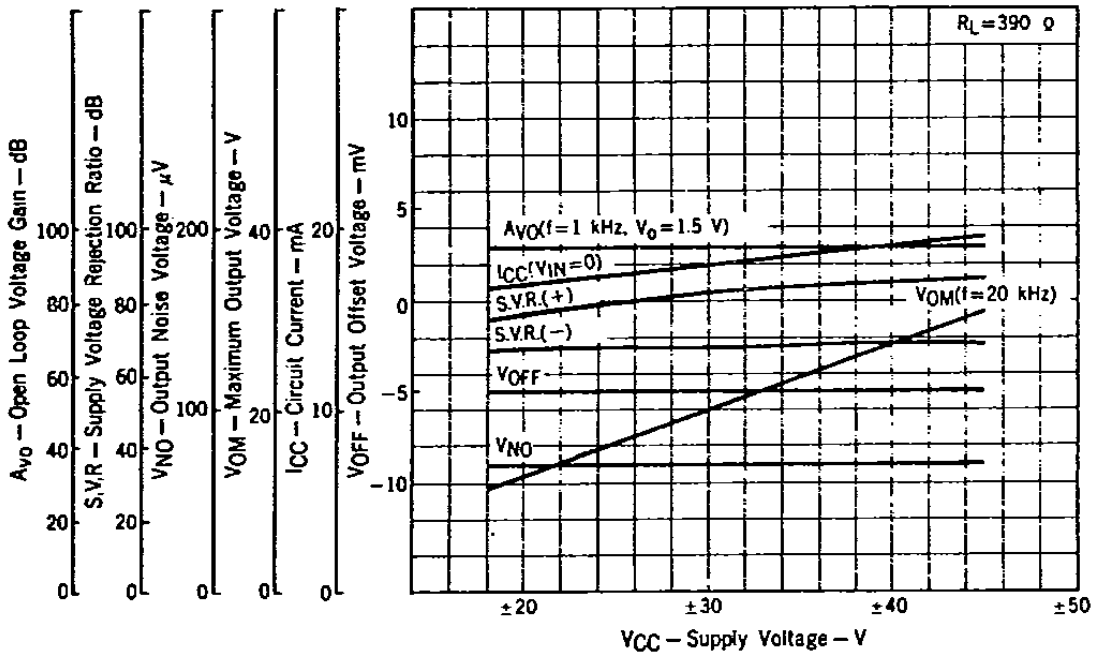
ALLOWABLE POWER DISSIPATION
vs. AMBIENT TEMPERATURE



VOLTAGE GAIN vs. FREQUENCY



OPEN LOOP VOLTAGE GAIN
SUPPLY VOLTAGE REJECTION RATIO
OUTPUT NOISE VOLTAGE
CIRCUIT CURRENT
OUTPUT OFFSET VOLTAGE
vs. SUPPLY VOLTAGE



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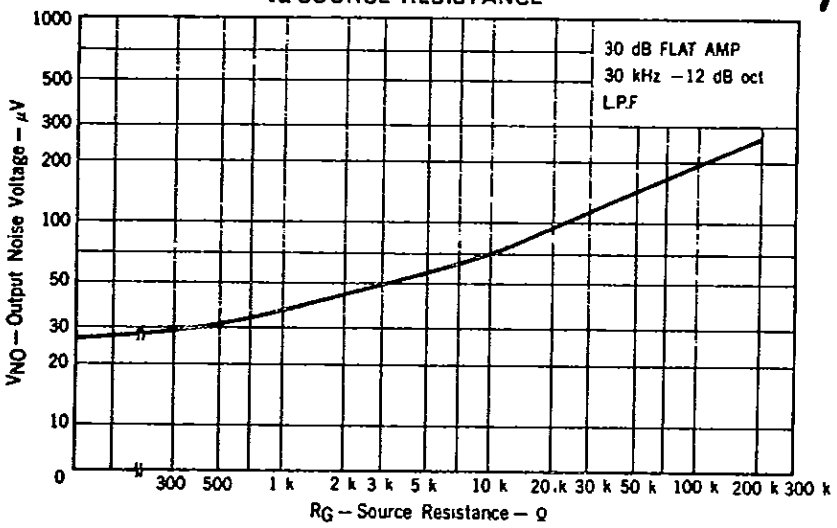
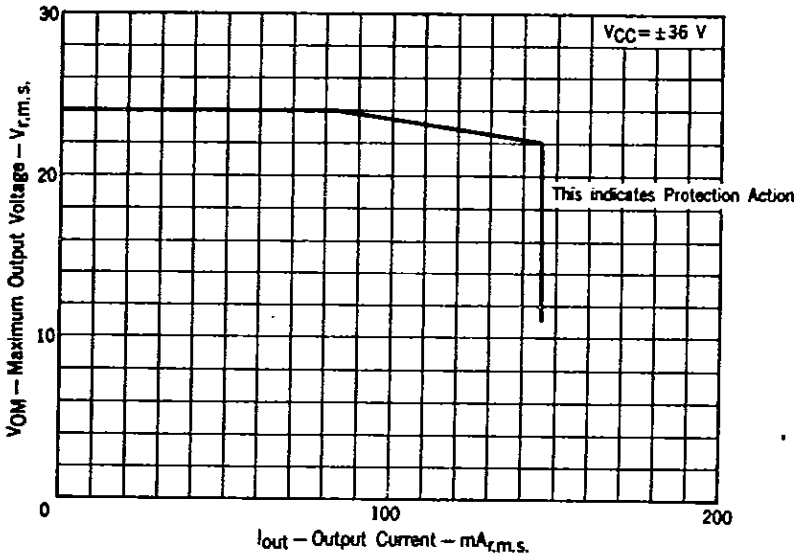
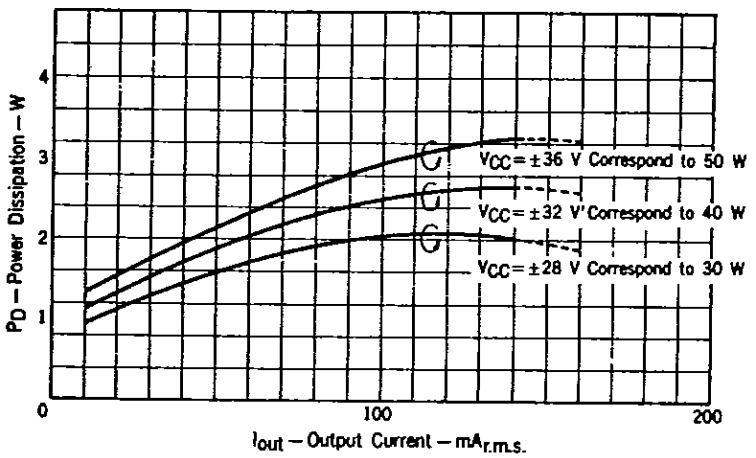
OUTPUT NOISE VOLTAGE
vs. SOURCE RESISTANCE



MAXIMUM OUTPUT VOLTAGE vs.
OUTPUT CURRENT



POWER DISSIPATION vs. OUTPUT CURRENT



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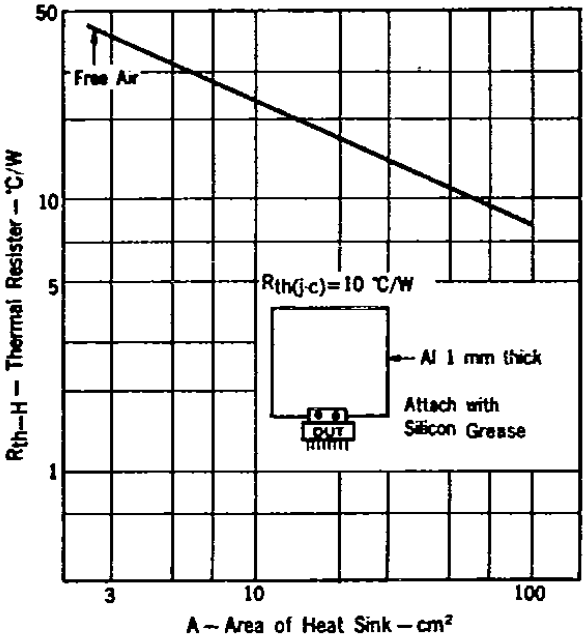
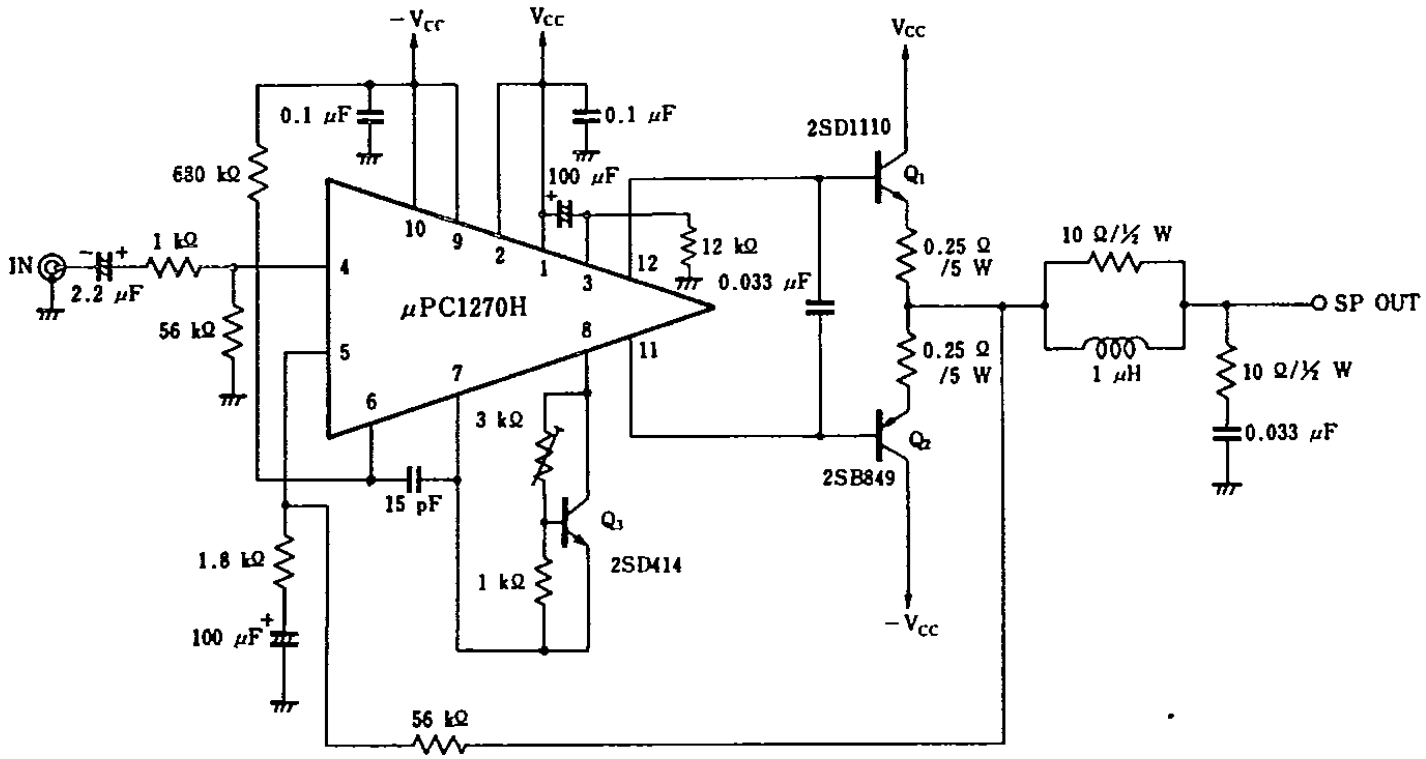
THERMAL RESISTER vs. AREA OF HEAT SINK



APPLICATION CIRCUIT-1



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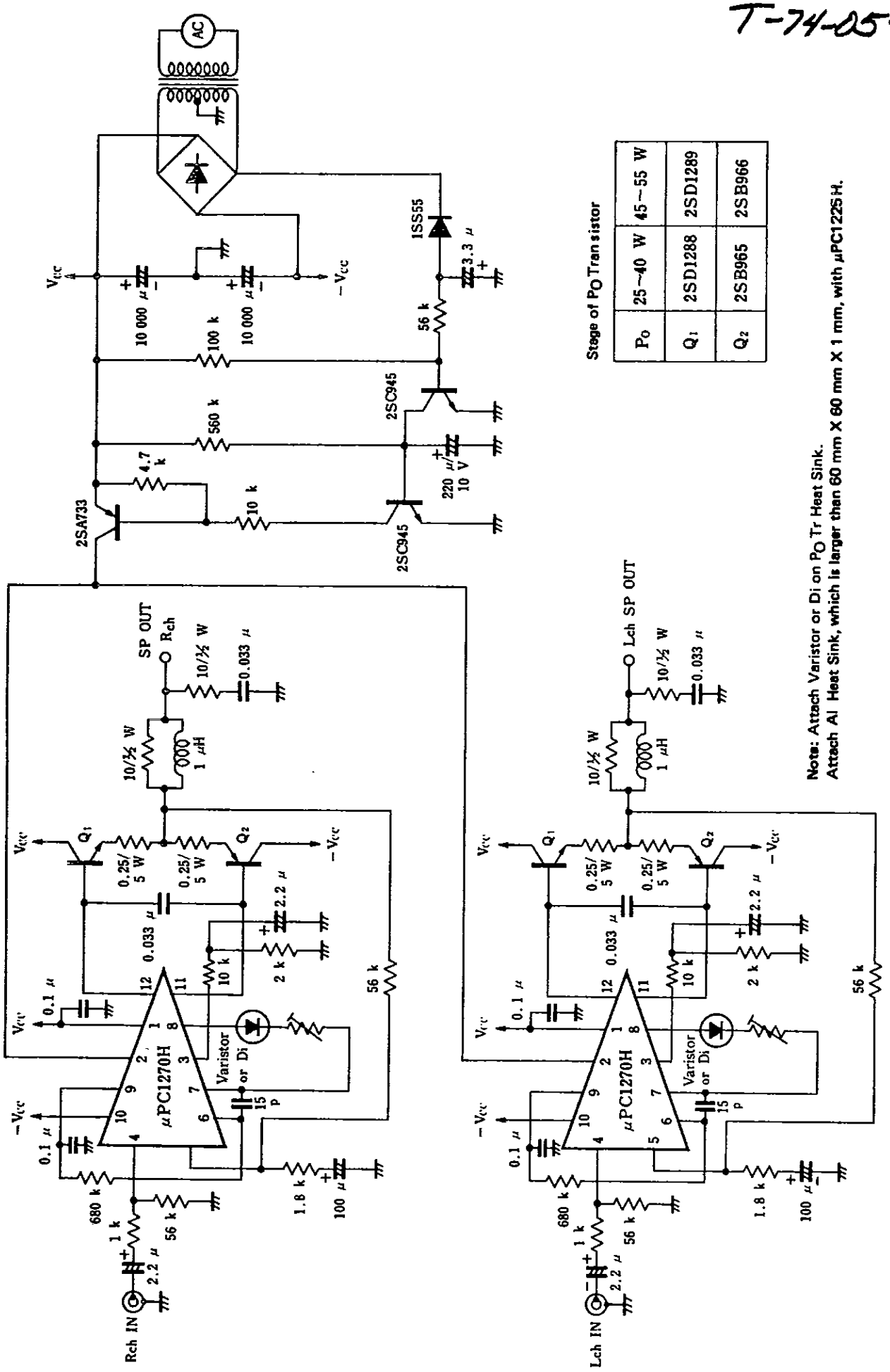
μPC1270H APPLICATION CIRCUIT-2 (no Relay)



Stage of P_O Transistor

P_O	25~40 W	45~55 W
Q_1	2SD1288	2SD1289
Q_2	2SB965	2SB966

Note: Attach Varistor or Di on P_O Tr Heat Sink.
Attach Al Heat Sink, which is larger than 60 mm X 60 mm X 1 mm, with μPC1225H.

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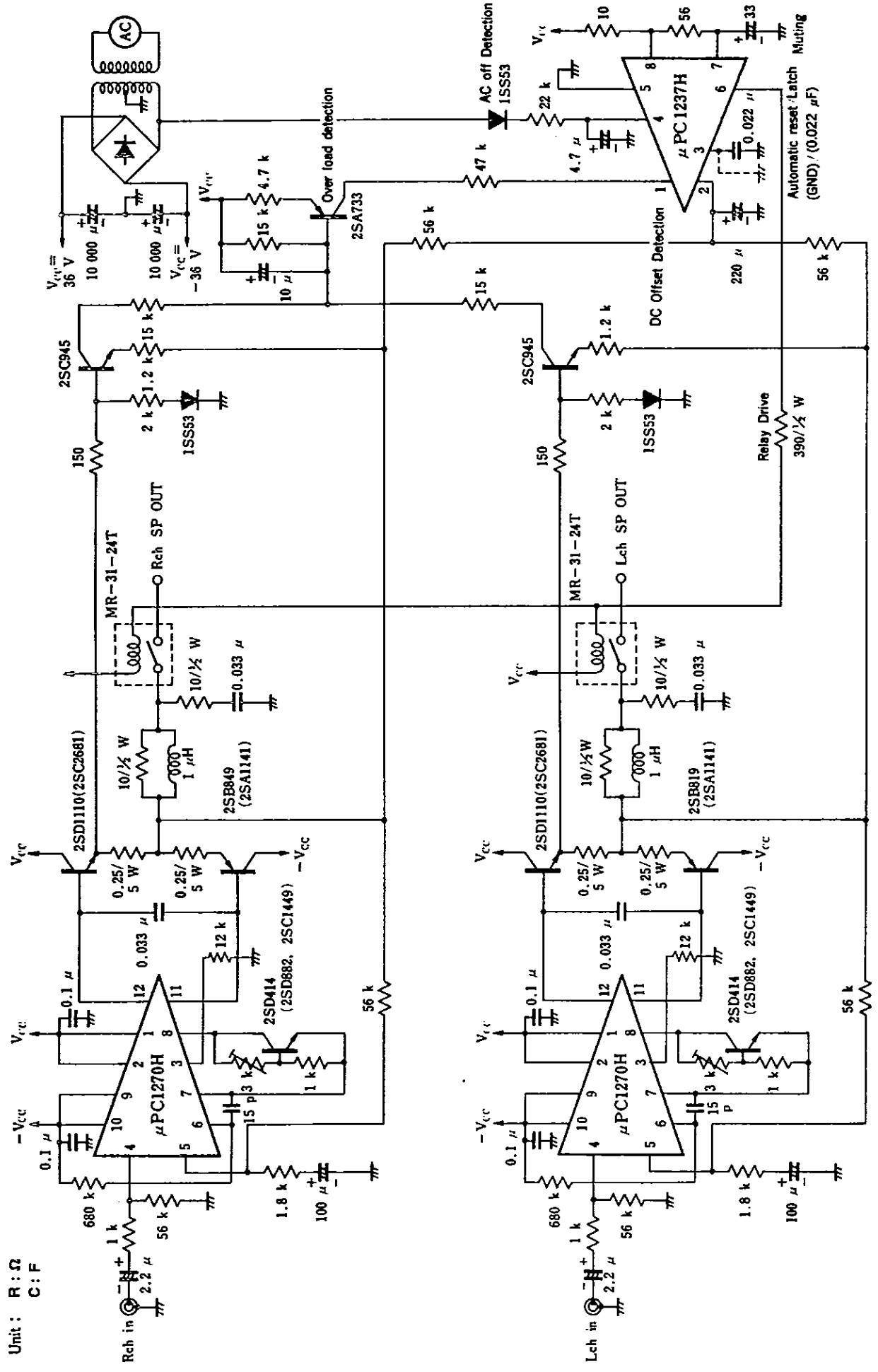
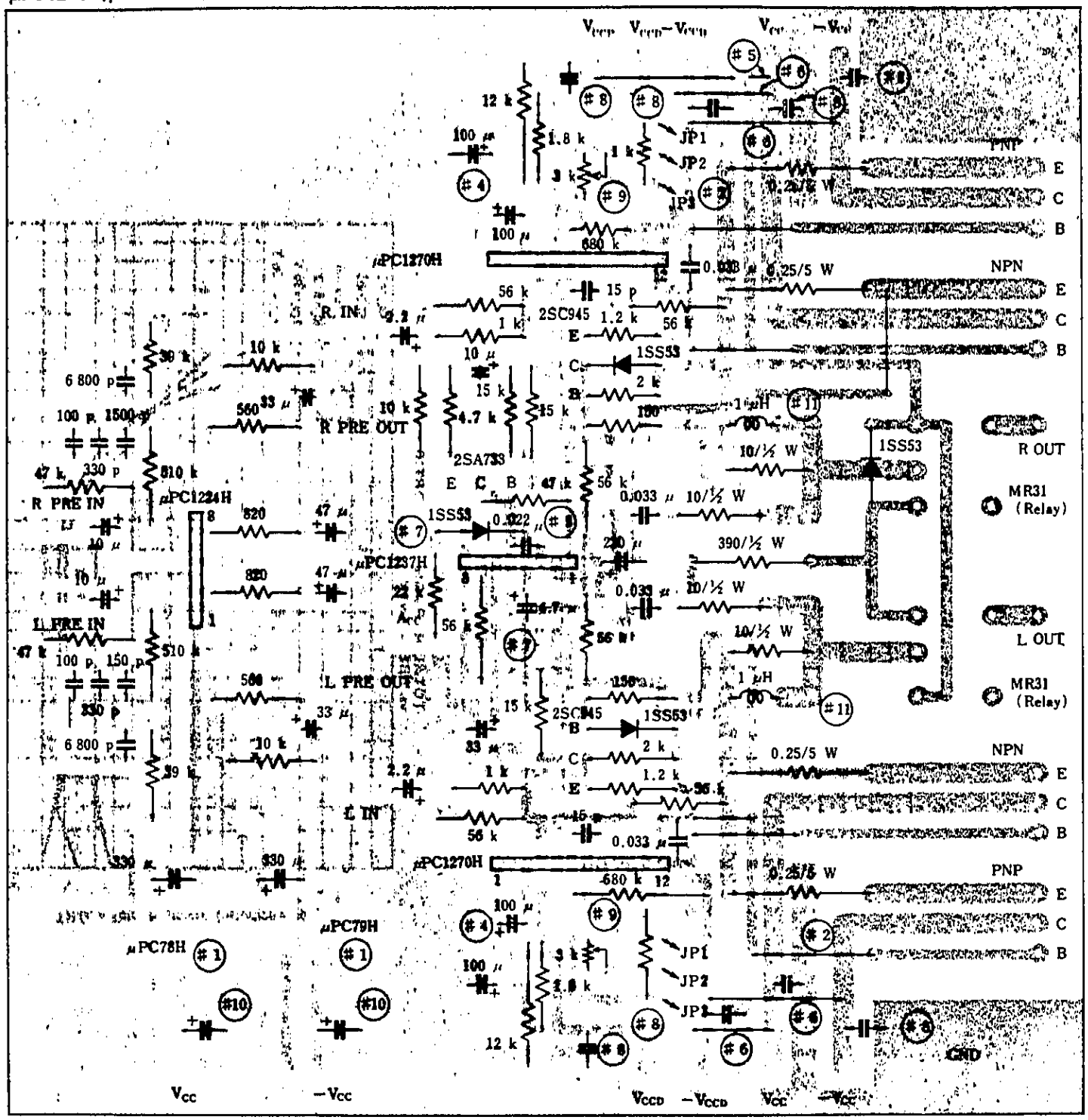
μPC1270H/μPC1237H/MP-80 EVALUATION CIRCUIT



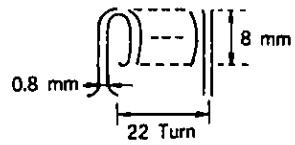
Note: Attach 2SD414 on P_D Tr Heat Sink.
Attach Al Heat Sink, which is larger than 60 mm X 60 mm X 1 mm, with μPC1270H.

μPC1270H/μPC1224H/MP-80 (2SC849, 2SD1110 or 2SA2681, 2SC1141) Evaluation Circuit Board Component Arrangement



Note:

- #1 These terminals are for 3-terminals regulators (μPC7818H, μPC7918H) as a μPC1224H power supply.
- #2 These terminals are for JP— lines to a temperature Compensation transistor (2SD414 or others).
- #3 Use 0.02 μF capacitance in case of using μPC1237H at latching function, while connect each other at automatic resetting.
- #4 This capacitance is for preventing POP ON/OFF noise. Thus, neglect it in case of using a relay.
- #5 These terminals are for JP—lines in case of using the same power supply (μPC1237H and Power Amplifier)
- #6 These terminals are for JP— lines in case of using the same power supply (μPC1270H and Power Tr)
- #7 This terminal is for AC-OFF Detection. Thus, use 8.2 k ohms instead of 22 k ohms, neglect 1SS53 and connect these 1SS53's terminals and neglect 4.7 μF in case of using DC power supply.
- #8 These capacitances are for preventing a parastic oscillation. Use a 0.1 μF.
- #9 These trimmers are for adjusting an idling current. Recommend Neo-Pot PS61 Series.
- #10 These capacitance are for the 3-terminals regulator input.
- #11 Design of 1 μH (example)



- #12 This indicates a copper board pattern

This is the evaluation circuit. Thus, it is not for a mass production considered about component deviation and the temperature characteristic.

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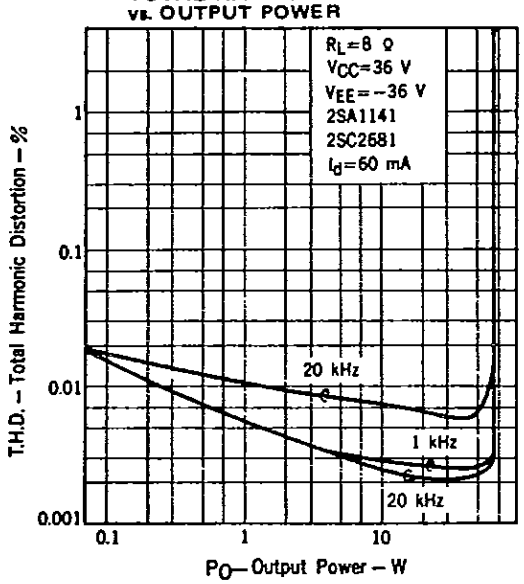
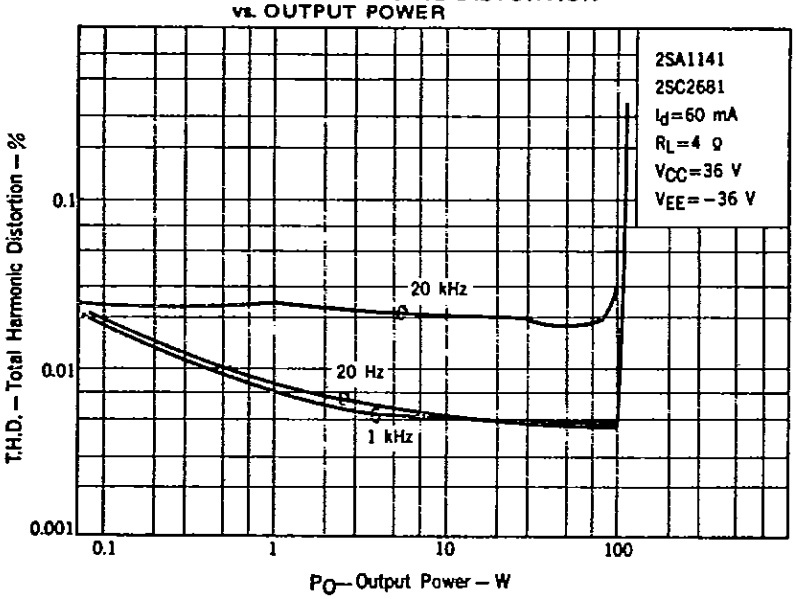
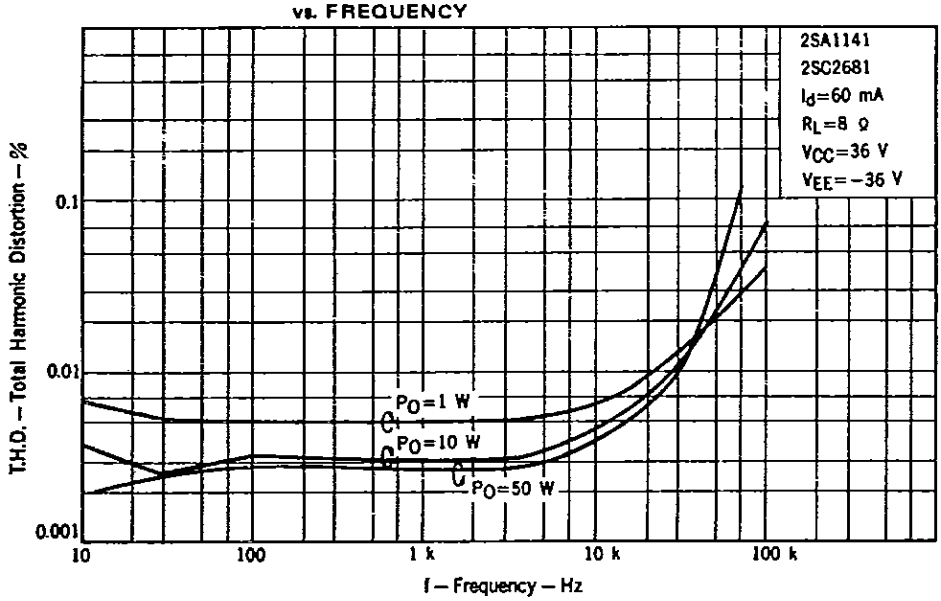
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



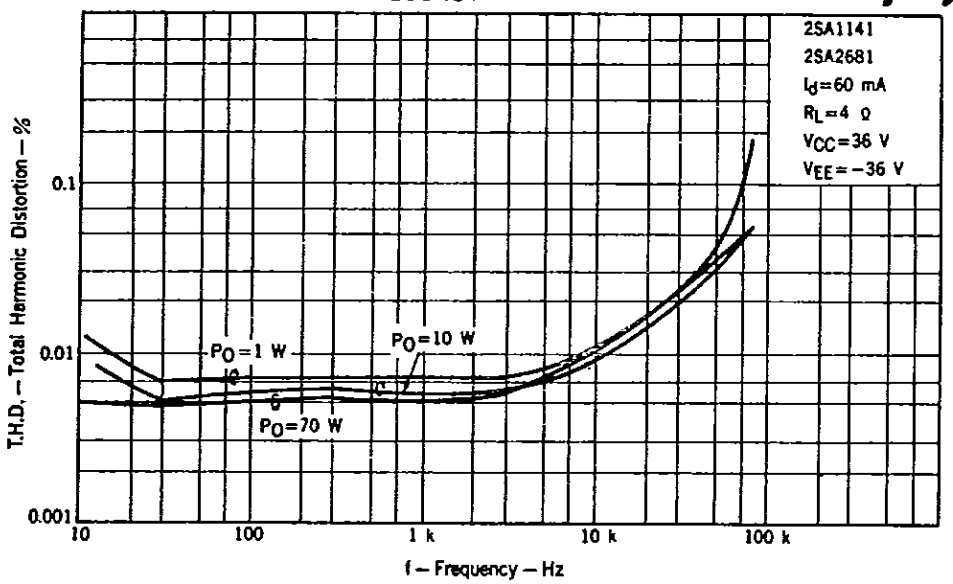
TOTAL HARMONIC DISTORTION
vs. OUTPUT POWER



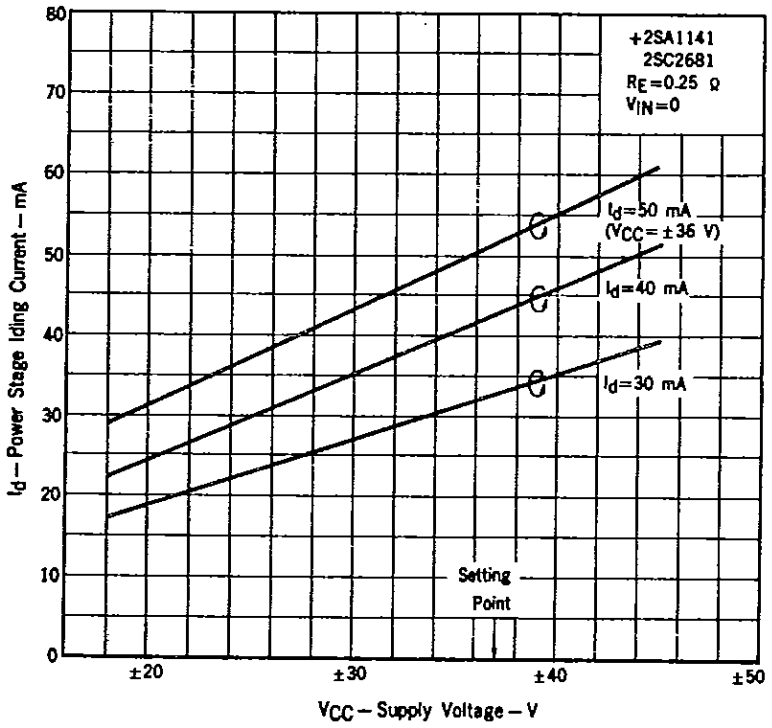
TOTAL HARMONIC DISTORTION
vs. FREQUENCY



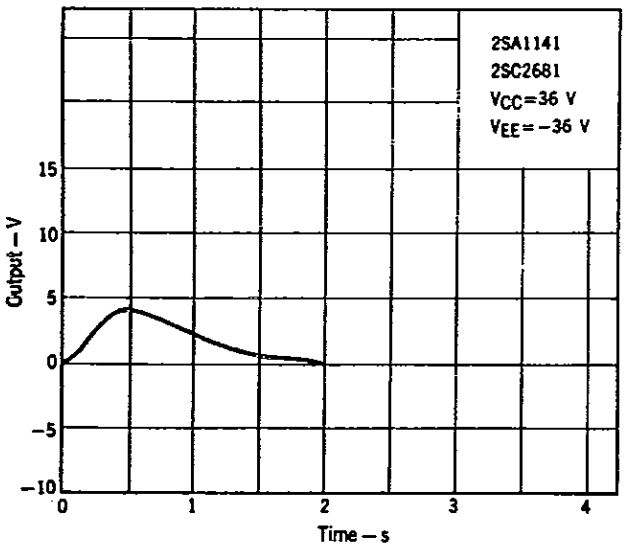
TOTAL HARMONIC DISTORTION
vs. FREQUENCY



POWER STAGE IDLING CURRENT
vs. SUPPLY VOLTAGE



POP NOISE (Sw on)



POP NOISE (Sw off)